

1 Colby B. Springer (214868)
2 cspringer@polsinelli.com
3 Hannah T. Yang (311814)
4 hyang@polsinelli.com
5 **POL SINELLI LLP**
6 Three Embarcadero Center
Suite 1350
San Francisco, California 94111
T: 415.248.2100
F: 415.248.2101

7 Attorneys for Plaintiff Anza Technology, Inc.

8 **UNITED STATES DISTRICT COURT**
9 **EASTERN DISTRICT OF CALIFORNIA**

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11 Anza Technology, Inc.
12 Plaintiff,
13 v.
14 Mushkin, Inc., a Colorado corporation, d/b/a
Mushkin Enhanced MFG.
15 Defendant.

Case No.

**COMPLAINT FOR
PATENT INFRINGEMENT**

DEMAND FOR JURY TRIAL

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18 Plaintiff Anza Technology, Inc. (“Anza” or “Plaintiff”), by and through its undersigned
19 counsel complains and alleges against Defendant Mushkin, Inc. d/b/a Mushkin Enhanced MFG
20 (“Defendant”) as follows:

21 **NATURE OF THE ACTION**
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23 1. This is a civil action for patent infringement arising under the laws of the United
24 States relating to patents, 35 U.S.C. § 101, et seq., including, without limitation, 35 U.S.C. §§
25 271 and 281. Plaintiff Anza seeks a preliminary and permanent injunction and monetary
26 damages for patent infringement.

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JURISDICTION AND VENUE

2. This court has subject matter jurisdiction over this case for patent infringement
3 under 28 U.S.C. §§ 1331 and 1338(a) and pursuant to the patent laws of the United States of
4 America, 35 U.S.C. § 101, *et seq.*

3. Venue properly lies within the Eastern District of California pursuant to the
7 provisions of 28 U.S.C. §§ 1391(b), (c), and (d) and 1400(b). On information and belief,
8 Defendant conducts substantial business directly and/or through third parties or agents in this
9 judicial district by selling and/or offering to sell the infringing products and/or by conducting
10 other business in this judicial district. Furthermore, Plaintiff is informed and believes that
11 Defendant engages in business in this district, and that Plaintiff has been harmed by Defendant's
12 conduct, business transactions and sales in this district.
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4. This Court has personal jurisdiction over Defendant because Defendant transacts
15 continuous and systematic retail business within the State of California. This Court has personal
16 jurisdiction over the Defendant because Plaintiff is informed and believes that this Defendant's
17 infringing activities, including, without limitation, the making, using, selling and/or offers for
18 sale of infringing products occur in the State of California. In particular, Defendant's infringing
19 products are sold at local retail stores within the District at, among others, Staples, Best Buy and
20 Target. Finally, this Court has personal jurisdiction over Defendant because, on information and
21 belief, Defendant has made, used, sold and/or offered for sale its infringing products and placed
22 such infringing products in the stream of interstate commerce with the expectation that such
23 infringing products would be made, used, sold and/or offered for sale within the State of
24 California.
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5. Upon information and belief, certain of the products manufactured by or for
27 Defendant have been and/or are currently designed and/or offered for sale by Defendant through
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1 an in-house sales and marketing team.
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PARTIES

5 6. Plaintiff Anza is a corporation organized and existing under the laws of the State
of California with an office and principal place of business at 4121 Citrus Avenue, Suite 4,
7 Rocklin, California 95677. Anza is a designer, manufacturer and seller of products directed to
8 the manufacture and assembly of electronics including the bonding of electrostatic-sensitive
9 devices.

10 7. Defendant is a corporation organized and existing under the laws of the State of
Colorado, with an office at 14 Inverness Drive East, Suite F-100, Englewood, Colorado 80112
11 with its principal place of business in the State of Texas at 828 New Meister Lane, Suite 300,
12 Pflugerville, Texas 78660. Defendant also maintains a registered agent in the State of California
13 at 29222 Rancho Viejo Road, Suite 203, San Juan Capistrano, California 92675.
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BACKGROUND

16 17 8. Defendant designs, manufactures, assembles or imports products with Integrated
Circuit (“IC”) chips. The IC chips are electrostatic discharge (“ESD”) sensitive devices.
18 Assembly of Defendant’s products with these ESD sensitive IC chips requires certain techniques
19 and methods to guard against ESD events that have catastrophic consequences on IC chips.
20 These certain techniques and methods infringe the Asserted Patent, described in further detail
21 below.
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24 9. ESD damage is a well-known phenomenon in the electronics industry and
25 broadly-accepted standards have been developed by industry-recognized standards-setting
26 organizations (such as ANSI, JEDEC, the IEC and/or the ESDA) (cumulatively “ESD-
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1 Standards") to minimize the risk of damage to ESD sensitive devices during assembly and
2 manufacture. Each of the aforementioned industry standards thus requires the use of
3 manufacturing tools made of dissipative materials having approximately the same resistance
4 values in connection with handling ICs that are particularly sensitive to ESD events. These
5 resistance ranges are low enough to prevent a discharge of a charge to an ESD sensitive device
6 such as the Accused Products, but high enough to avoid current flows that may damage the
7 device.

9 10. Failing to adhere to such standards could otherwise lead to ESD events during the
10 bonding process that could damage the ICs and render them defective and/or unusable. Today, as
11 little as five volts of an ESD event is enough to permanently change the structures in ESD
12 sensitive devices, which include, but are not limited to, ICs, Printed Circuit Boards ("PCBs") and
13 other electronic components.
14

15 11. Complementary Metal-Oxide Semiconductors ("CMOS") are a type of IC
16 commonly used in microprocessors, microcontrollers, static RAM and other digital logic circuits.
17 CMOS ICs are known to be ESD sensitive and are highly susceptible to damage caused by ESD
18 events.
19

20 12. CMOS chips are typically cut from a wafer of silicon into individual pieces,
21 called "dies." The die is picked up by a tool and placed on a substrate or package for placement
22 on a PCB as shown below in Fig 1.
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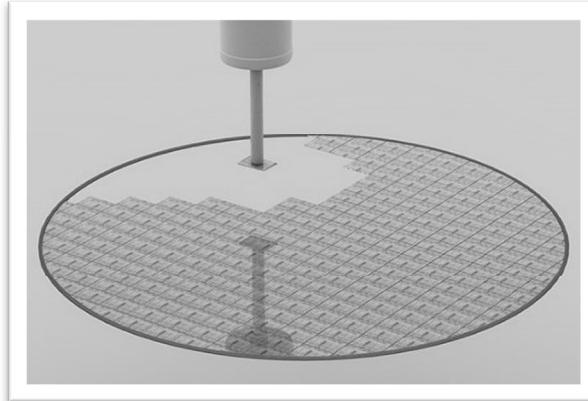


Figure 1. Die picked up by tool.

13. A common method of packaging CMOS ICs for handling and mounting on PCBs
14. is the Ball Grid Array mounting system (or a variation thereof *e.g.* FBGA, TBGA, PBGA)
15. (cumulatively referred to herein as “BGA”). An individual CMOS IC wafer is inserted in a
16. package that uses “solder balls” as conduits of electrical connectivity. ICs with BGA mounting
17. packages are thereafter surface mounted to PCBs via the array of solder balls.

18. 14. Flip chip bonding techniques are commonly used in fabricating BGA packaged
19. ICs and in placing BGA components on PCBs. Flip chip microelectronic assembly is the direct
20. electronic connection of facedown electronic components onto substrates, circuit boards, or
21. carriers by means of conductive bumps on the BGA IC package.

22. 15. During the process of bonding a BGA IC to a PCB, the IC comes in contact with
23. tools that place it on the PCB with the solder balls facing down. Heat is then applied causing the
24. solder balls to melt resulting in the bonding of the IC and BGA package to the surface of the
25. PCB. Naturally occurring electrostatic charges (of varying degrees) build up when the mounting
26. tools come in contact with the die and when it is placed in the package. Electrostatic charges can
27. also build up when the die in the BGA package is placed in a tray or on a tape for transport, and
28. also when it is removed from the transport vessel and placed on a PCB for bonding.

16. Essentially, every time an ESD sensitive device is handled, electrostatic charges

to one degree or another are generated. Any type of movement can charge an ESD sensitive device. Tribocharging, for example, commonly occurs in automated assembly lines with the rubbing of conveyor belts, or when ICs and product parts touch carrier trays or tapes. Electrostatic charges are therefore created at several places in an automated production line including but not limited to 1) during the application of conductive material, 2) during pickup and placement of ICs, and 3) during testing of the assembled devices.

17. Since automated production line processes generate electrostatic charges, caution has to be taken to avoid damaging ESD sensitive components when they are moved, picked up and placed in contact with one another. For these reasons, ESD sensitive devices that come in contact with automated handling equipment during the manufacture of the Accused Products should be made of electrostatic dissipative material and a resistance to ground where the ESD sensitive devices are contacted.

18. As a result, Plaintiff is informed, believes and thereon alleges that the Defendant uses specific design, engineering and manufacturing practices in making the Accused Products to minimize the costs resulting from damaging ESD events. Further, Plaintiff alleges that Defendant specifies and/or directs that the Accused Products be assembled or manufactured in ways that meet or exceed ESD-Standards for reducing the risk of damage to ESD sensitive devices.

ACCUSED PRODUCTS

19. The Accused Products for purposes of the asserted patent include but are not limited to BGA packaged ICs and PCBs that to which the BGA packaged ICs are mounted. The Accused Products therefore include but are not limited to the following BGA packaged ICs: REDLINE, BLACKLINE, RADIOACTIVE, STEALTH, SILVERLINE, PROLINE, ESSENTIALS, NOTEBOOK MEMORY, STRIKER, REACTOR, TRIACTOR, CHRONOS,

CATALYST, PROSPEC, ATLAS, and SCORPION (the "Accused Products").

20. The Accused Products utilize BGA ICs that are bonded to PCBs. As explained above, in order to minimize the risk of an ESD event, BGA-packaged ICs are manufactured using processes and methods that infringe at least independent claims 1, 14, and 16 of the '927 patent. Therefore, Plaintiff is informed, believes and thereon alleges that Defendant specifies the use of BGA ICs for use in the Accused Products. Plaintiff is further informed, believes and thereon alleges that the Accused Products are manufactured on assembly lines that utilize processes and methods taught by independent claims 1, 14, and 16 of the '927 patent to reduce the risk of damage from ESD events.

21. Furthermore, the ICs in the Accused Products are highly sensitive to ESD events as evidenced by the charge load tolerance specifications promulgated by their manufacturers.

THE ASSERTED PATENT

22. On October 24, 2006, the United States Patent and Trademark Office (“USPTO”) duly and legally issued United States Patent No. 7,124,927 entitled “FLIP CHIP BONDING TOOL and BALL PLACEMENT CAPILLARY” (the “’927 patent”). Steven F. Reiber is the patent’s sole named inventor and Plaintiff is owner, by assignment, of the entire right, title and interest in and to the ’927 patent and vested with the right to bring this suit for damages and other relief. A true and correct copy of the ’927 patent is attached hereto as Exhibit A.

COUNT ONE

INFRINGEMENT OF THE '927 PATENT BY DEFENDANT

23. Plaintiff re-alleges and incorporates by reference each of the allegations set forth in paragraphs 1 through 22 above.

1 24. Defendant has, since at least the filing of this complaint, had knowledge of
2 infringement of the '927 patent.

3 25. Plaintiff is informed, believes and thereon alleges that the Accused Products
4 directly, or alternatively under the doctrine of equivalents, infringe each of the limitations of
5 independent claims 1, 14, and 16 of the '927 patent in violation of 35 U.S.C. § 271(a) and (g)
6 when Defendant imports into the United States or offers to sell, sells, or uses within the United
7 States a product which is made by the processes described herein. Defendant also violates 35
8 U.S.C. § 271(a) to the extent that it conducts such infringing activity in the territory of the United
9 States.

10 26. Furthermore, Defendant purports to be a JEDEC Member, claiming that “[its] in-
11 house engineers utilize JEDEC . . . to build innovative module solutions that match today’s
12 computer performance standards.” See Mushkin Certifications webpage, attached hereto as
13 Exhibit B. Plaintiff is therefore informed, believes and thereon alleges that Defendant and/or its
14 contract manufacturer assembles the Accused Products, in compliance with one or more ESD-
15 Standards, such as JEDEC, which employs a method of ESD control that infringes independent
16 claims 1, 14, and 16 of the '927 patent. On information and belief, Defendant specifies that BGA
17 ICs are used in the Accused Products.

18 27. In following conventional industry practices, tools are used in the process of
19 manufacturing or assembling the Accused Products to surface mount and bond BGA ICs to
20 PCBs. Plaintiff is informed and believes and thereon alleges that during the assembly or
21 manufacture of the Accused Product, the Defendant or its contract manufacturer uses tools with
22 tips that are specially designed to reduce the risk of damage to BGA ICs from ESD events.
23 Specifically, Plaintiff is informed, believes and thereon alleges that Defendant complies with
24 reasonable and prudent ESD-Standard practices and techniques in the manufacture or assembly
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1 of the Accused Products to reduce the risk of ESD events through the use of electrically
2 dissipative tool tips, which reduce sudden discharges of electrostatic current into the BGA ICs
3 that are being bonded to PCBs in the Accused Products, as taught by independent claims 1, 14,
4 and 16 of the '927 patent.
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7 **PRAYER FOR RELIEF**

8 **WHEREFORE**, Plaintiff prays for relief and judgment as follows:

- 9 1. That Defendant has infringed the Patent-in-Suit;
10 2. Compensation for all damages caused by Defendant's infringement of the Patent-
11 in-Suit to be determined at trial;
12 3. A finding that this case is exceptional and an award of reasonable attorneys fees
13 pursuant to 35 U.S.C. § 285;
14 4. Granting Plaintiff pre-and post-judgment interest on its damages, together with all
15 costs and expenses; and,
16 5. Awarding such other relief as this Court may deem just and proper.

17 **DEMAND FOR JURY TRIAL**
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19 Plaintiff hereby demands a trial by jury on all claims.
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1 Dated: March 28, 2017

POLSINELLI LLP

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3 By: /s/ Colby B. Springer
4 Colby B. Springer (SBN 214868)
5 cspringer@polsinelli.com
6 Hannah T. Yang (SBN 311814)
7 hyang@polsinelli.com
8 Three Embarcadero Center
9 Suite 1350
10 San Francisco, CA 94111

11 Attorneys for Plaintiff
12 ANZA TECHNOLOGY, INC.

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